UNI EN ISO 9001

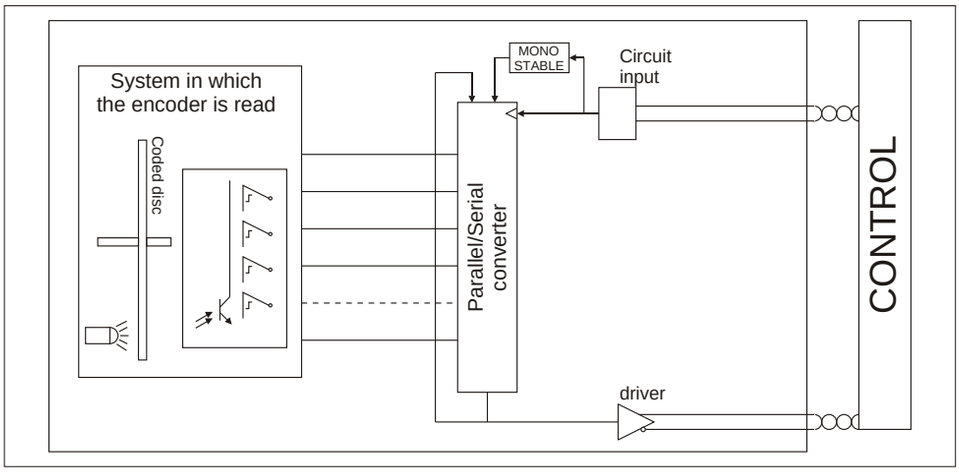
SSI
INTERFACE
GENERAL DESCRIPTION

Introdution

Continual evolution in the automation field has led to a continuous and growing requirement for precision in measurement devices and therefore also in absolute encoders. To satisfy these demands, absolute encoders have been created with high resolution. These however have the problem of needing a number of wires that grows with the number of bits and with the accuracy. To try to reduce installation costs and to simplify the wiring, the SSI interface was created. This performs the measurement data transmission in serial mode, usually using only two signals (CLOCK and DATA), independently of encoder accuracy.

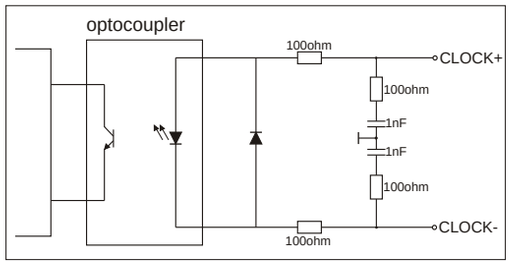
Description

The SSI interface permits the transfer of the absolute encoder position information through a serial line, synchronised with a clock. The following figure shows the block diagram of an encoder with an SSI interface:

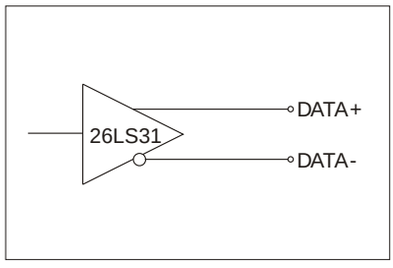


The encoder with an SSI interface is constituted by the classic absolute encoder position measurement system including: a light source, a disc with transparent and opaque zones, photo-electric receivers, comparison/trigger circuits, a parallel/serial converter, a mono-stable circuit, an input circuit for the clock signal and by an output driver for the data signal.

The value of the position is taken by the encoder reading system and continually sent to a parallel/serial converter (constituted essentially of a “shift register” with parallel loading). When the mono-stable circuit is activated by a clock signal transition, the data is memorised and sent to the output, scheduled according to the clock's own signal. The CLOCK and DATA signals are transmitted differentially (RS422) to increase immunity from interference and to be able to support long transmission distances.



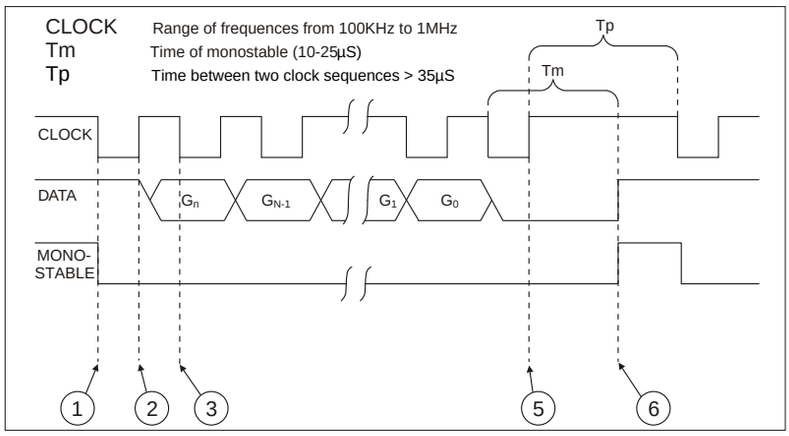
CLOCK signal circuit input



DATA signal circuit output

Operating principle

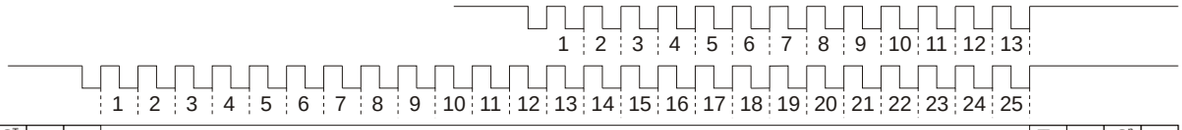
In rest conditions, the CLOCK and DATA lines are at a high logical level and the mono-stable circuit is disabled (high level).



1. On the first CLOCK signal descent front, the mono-stable is activated and the parallel value present at the input to the P/S converter is memorised in the shift register.
2. On the CLOCK signal ascent front, the most significant bit (MSB) is placed in the output on the DATA line.
3. On the CLOCK descent front when the signal is stable the controller acquires the level from the DATA line, which is the value of the most significant bit, the mono-stable is re-activated.
4. On each further ascent front of the CLOCK impulse sequence, the successive bits up to the least significant one are place in the output on the DATA line and acquired by the control on the descent front.
5. At the end of the CLOCK impulse sequence when the external control has also acquired the value of the least significant (LSB) the CLOCK impulse sequence is interrupted and therefore the mono-stable is no longer re-activated.
6. Once the mono-stable time (Tm) has elapsed, the DATA line returns to a high logical level and the mono-stable disables itself.

Transmission protocol

The frame length of the transmitted data depends only on the type of encoder (single turn or multi-turn) and not on the total number of encoder bits. In fact, the standard frame length for a single turn encoder is 13 bits, whilst for a multi-turn one it is 25 bits. The alignment of the significant data inside the frame is at the centre, as shown by the table below:



T	2^T																									Ta		2^n	n
12	4096	1	1	G_{n+11}	G_{n+10}	G_{n+9}	G_{n+8}	G_{n+7}	G_{n+6}	G_{n+5}	G_{n+4}	G_{n+3}	G_{n+2}	G_{n+1}	G_n	G_{n-1}	G_{n-2}	G_{n-3}	G_{n-4}	G_{n-5}	G_{n-6}	G_{n-7}	G_{n-8}	G_{n-9}	G_{n-10}	G_{n-11}	G_{n-12}	G_{n-13}	0	1	8192	13
11	2048	1	1	0	G_{n+10}	G_{n+9}	G_{n+8}	G_{n+7}	G_{n+6}	G_{n+5}	G_{n+4}	G_{n+3}	G_{n+2}	G_{n+1}	G_n	G_{n-1}	G_{n-2}	G_{n-3}	G_{n-4}	G_{n-5}	G_{n-6}	G_{n-7}	G_{n-8}	G_{n-9}	G_{n-10}	G_{n-11}	G_{n-12}	0	0	1	4096	12
10	1024	1	1	0	0	G_{n+9}	G_{n+8}	G_{n+7}	G_{n+6}	G_{n+5}	G_{n+4}	G_{n+3}	G_{n+2}	G_{n+1}	G_n	G_{n-1}	G_{n-2}	G_{n-3}	G_{n-4}	G_{n-5}	G_{n-6}	G_{n-7}	G_{n-8}	G_{n-9}	G_{n-10}	G_{n-11}	0	0	0	1	2048	11
9	512	1	1	0	0	0	G_{n+8}	G_{n+7}	G_{n+6}	G_{n+5}	G_{n+4}	G_{n+3}	G_{n+2}	G_{n+1}	G_n	G_{n-1}	G_{n-2}	G_{n-3}	G_{n-4}	G_{n-5}	G_{n-6}	G_{n-7}	G_{n-8}	G_{n-9}	G_{n-10}	0	0	0	0	1	1024	10
8	256	1	1	0	0	0	0	G_{n+7}	G_{n+6}	G_{n+5}	G_{n+4}	G_{n+3}	G_{n+2}	G_{n+1}	G_n	G_{n-1}	G_{n-2}	G_{n-3}	G_{n-4}	G_{n-5}	G_{n-6}	G_{n-7}	G_{n-8}	G_{n-9}	0	0	0	0	0	1	512	9
7	128	1	1	0	0	0	0	0	G_{n+6}	G_{n+5}	G_{n+4}	G_{n+3}	G_{n+2}	G_{n+1}	G_n	G_{n-1}	G_{n-2}	G_{n-3}	G_{n-4}	G_{n-5}	G_{n-6}	G_{n-7}	G_{n-8}	0	0	0	0	0	0	1	256	8
6	64	1	1	0	0	0	0	0	0	G_{n+5}	G_{n+4}	G_{n+3}	G_{n+2}	G_{n+1}	G_n	G_{n-1}	G_{n-2}	G_{n-3}	G_{n-4}	G_{n-5}	G_{n-6}	G_{n-7}	0	0	0	0	0	0	0	1	128	7
5	32	1	1	0	0	0	0	0	0	0	G_{n+4}	G_{n+3}	G_{n+2}	G_{n+1}	G_n	G_{n-1}	G_{n-2}	G_{n-3}	G_{n-4}	G_{n-5}	G_{n-6}	0	0	0	0	0	0	0	0	1	64	6
4	16	1	1	0	0	0	0	0	0	0	0	G_{n+3}	G_{n+2}	G_{n+1}	G_n	G_{n-1}	G_{n-2}	G_{n-3}	G_{n-4}	G_{n-5}	0	0	0	0	0	0	0	0	0	1	32	5
3	8	1	1	0	0	0	0	0	0	0	0	0	G_{n+2}	G_{n+1}	G_n	G_{n-1}	G_{n-2}	G_{n-3}	G_{n-4}	0	0	0	0	0	0	0	0	0	0	1	16	4
2	4	1	1	0	0	0	0	0	0	0	0	0	0	G_{n+1}	G_n	G_{n-1}	G_{n-2}	G_{n-3}	0	0	0	0	0	0	0	0	0	0	0	1	8	3
1	2	1	1	0	0	0	0	0	0	0	0	0	0	0	G_n	G_{n-1}	G_{n-2}	0	0	0	0	0	0	0	0	0	0	0	0	1	4	2

Singleturn

Multiturn

Number of turns

Position/turn

The format of the frame transmitted depends on the configuration of the encoder concerning the number of bits per turn and the number of bits for the turns.
n = number of bits on the turn
T = number of bits for the turns

Ta = $Tm - \frac{Tc}{2}$
Tc= clock period
Tm= monoflop time

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